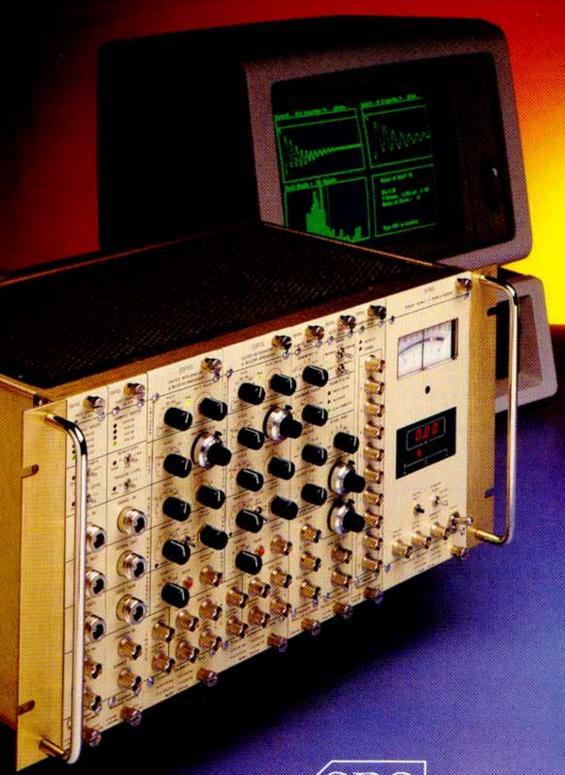
Fast Gated Integrators and Boxcar Averagers



SRS

STANFORD RESEARCH SYSTEMS

The System

The Stanford Research Systems' Gated Integrator and Boxcar Averager System is a versatile instrument designed to recover and process fast analog signals. The system consists of a NIM-compatible mainframe and modules which can be selected to tailor the system to your specific needs.

Compatibility

The system mainframe provides regulated power to each of the modules. Because the mainframe is NIM compatible, you are able to use modules from other manufacturers or ones that you build yourself. A wide variety of modules are available in the NIM format including amplifiers, counters, discriminators, and pulse height analyzers. Each of the SRS modules is NIM compatible and may be used in NIM standard crates from other manufacturers.

Versatility

The Boxcar System has been designed to operate in a wide range of configurations:

- 1. Stand-alone analog data acquisition.
- Interfaced to virtually any computer via the RS-232 or GPIB interfaces, or to the computer's A/D and D/As.
- "Turn-key" data acquisition, storage, graphics and analysis on IBM PC or compatible computers using SRS application programs.

Convenient, Simple Operation

Unlike other boxcar averagers, this one is easy to operate. Look at the front panel of the Gated Integrator Module—operation of this unit is very simple. For example, you specify the boxcar averaging in number of samples, and the

Gate Output lets you see the exact (±1 nS) position of the sample gate with respect to the input signal. No guesswork is involved.

Shot by Shot

An important feature of the Gated Integrator and Fast Sampler Modules is the Last Sample Output. The analog voltage at this output is proportional to the average of the input signal during the most recent gate. This output may be digitized by the computer interface module to allow shot-by-shot analysis of the experimental data.

Computer Interface and PC Software

The SR245 Computer Interface Module provides 12 Bit A/D and D/A at eight analog input/output ports. The module allows your computer to read outputs from your gated integrator, to scan gates, and to interface with other analog or digital equipment in your lab.

While the SR245 can operate with virtually any computer via its RS-232 and GPIB interfaces, a complete data acquisition package for IBM PC computers is also available.

The Solution

The Stanford Research Systems Boxcar Averager System is the answer to your fast analog data acquisition problems. The system provides the speed, accuracy, flexibility and convenience that are needed in your research laboratory.

Model SR250 Gated Integrator

The Model SR250 Gated Integrator and Boxcar Averager is a versatile, high speed, low cost NIM module designed to recover fast analog signals from noisy backgrounds.

The SR250 consists of a gate generator, a fast gated integrator, and exponential averaging circuitry. The gate generator, triggered internally or externally, provides an adjustable delay from a few nanoseconds to 100 milliseconds, before it generates a continuously adjustable gate from 2 nanoseconds to 15 microseconds (a minor modification allows gates to $150\mu s$). The delay may be set by a front panel potentiometer, or automatically scanned by a rear panel input voltage in order to record entire waveforms.

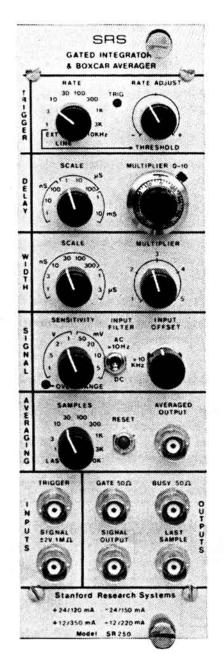
The fast gated integrator integrates the input signal during the gate. The output from the integrator is then normalized by the gate width to provide a voltage which is proportional to the average of the input signal during the sampling gate. This signal is further amplified (according to the front panel sensitivity setting) and then sampled by a low droop sample and hold amplifier, and output via a front panel BNC connector. This LAST SAMPLE output allows the experimenter to do a shot-by-shot analysis of the signal being studied, and makes the instrument a particularly useful component in a computer data acquisition system.

In addition to the traditional boxcar averaging technique, the averaging circuitry may be used to actively subtract a baseline drift or background from the signal of interest. This is accomplished by taking input samples at twice the experiment's repetition rate, inverting the baseline sample acquired when the signal is not present, and adding it to the moving average. This method of canceling baseline drift is analogous to phase sensitive detection which is used in frequency domain measurements.

Model SR250 Gated Integrator and Boxcar Averager

FEATURES

- Gate Widths from 2 nsec to 15 μsec (expandable to 150 μsec)
- Independent rate generator, gate control, and averaging
- Shot-by-Shot Output
- Trigger to gate delay < 25 nsec
- Low drift . . . < 0.5 mV/hr
- Jitter less than 20 psec + 0.01%
- Active Baseline Subtraction
- Gate Out shows precise timing
- DC to 20 KHz repetition rate
- Inputs protected to 100 VDC
- Average 1 to 10,000 samples



SPECIFICATIONS

TIMING CIRCUITS

Trigger Int: 0.5 Hz to 20 KHz, Single Shot, or Line.

Ext: ± 0.5 to $\pm 2V$. 5 nS minimum pulse. 1 M Ohm input impedance, protected to 100 VDC. Max trig rate=1/(50 μ S+Width+Delay+Full Scale Delay).

Delay Gate Delay = $25 \text{ nS} + (\text{Delay Range}) \times (\text{Delay Range})$

Multiplier). Accuracy is 2 nS or 5% of the full scale delay. Jitter is less than 20 pS or 0.01% of full scale. Gate Delay may be scanned by a rear panel input.

(0-10 volts gives 0-100% of full scale delay.)

Width Gate Width=(Width Scale)×(Width Multiplier).

Gate Width: 2 nS-15 µS (150 µS with modification).

200 mV pulse shows the position of the sample gate with respect to the Signal Output with 1 nS accuracy.

TTL Output goes high from the trigger until ready for the next trigger. Busy time is approximately

50 µS+Delay+Width+Full Scale Delay.

SIGNAL CHANNEL

Gate Output

Busy Output

Signal Input Zin=1 M Ohm. (50 Ohms with Signal Out

Terminated). Input Offset Drift <0.5 mV/hr. Shot noise <0.5 mVrms. Coherent Pickup: <8 mV in first 100 nS, <1 mV after 100 nS, <100 μ V when using

Baseline Subtraction.

Signal Filter DC, AC above 10 Hz, or AC above 10 KHz.

Sensitivity (Volts Out)/(Volts In) from 1 V/V to 1 V/5 mV in a

1,2,5 sequence.

Accuracy ±3% for gate widths greater than 10 nS. Sensitivity

decreases to about 50% at 2 nS gate width.

Offset 10 turn control adds offsets of ± 0.4 V to the input.

The offset may need adjustment when the gate width

is changed.

OUTPUTS

Last Sample ±10 VDC full scale. Polarity set on rear panel.

Output Impedance <1 Ohm with 10 mA drive capacity.

Oncop <0.2% of full scale per second.

Responsivity >95% (no more than 5% of the previous sample

remains).

Average Out Exponential moving average over 1 to 10,000 samples.

May be reset by pushbutton or logic input. ±10 V full

scale, polarity set on rear panel.

Output Impedance <1 Ohm with 10 mA drive capacity.

Droop <1%/minute on 1 to 30 samples, <0.01%/minute on

100 to 10,000 samples. All droop errors <1% of full

scale for trigger rates greater than 1 Hz.

GENERAL SPECIFICATIONS

Power +24V/120 mA, +12V/350 mA, -12V/220 mA,

-24V/150 mA. About 14 Watts total. Power from a NIM-standard crate or from SRS NIM mainframe

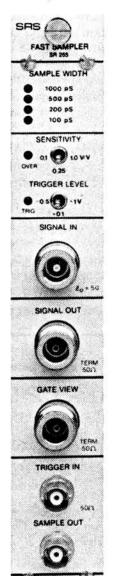
model SR280.

SR255 Fast Sampler Module

The SR255 Fast Sampler is an important tool for short pulse duration experiments. It provides four user-selectable gate widths from 100 psec to 1 nsec. All of the electronics are built into the module including A/D, D/A and a PROM correction circuit to eliminate the inherent non-linearities in the sampling bridge. Output is provided in both digital and analog form. Input sensitivity can be set from 100 mV/V to 1 V/V and trigger level selection is provided for broad trigger source compatibility. The gate view allows you to see precisely when the sample is being taken. The gate can be scanned by a rear panel voltage input from the SR200 Gate Scanner or SR245 Computer Interface. The signal out aids in sample timing and special applications such as time domain reflectometry or shorted-cable baseline subtraction. This module can be used alone, combined with the SR245 Computer Interface Module for computer data acquisition, or operated with the SR200 Gate Scanner for waveform recovery.

FEATURES

- Gate Widths from 100 psec to 1 nS
- Droopless analog output
- Linear over full range
- Jitter less than 2 psec rms
- 20 nsec trigger to gate delay
- Trigger rates up to 50 KHz



SPECIFICATIONS

TIMING CIRCUITS

BNC, 50 Ohm termination. Trigger Input

Thresholds: -0.5, +0.1, or +1 VDC.

Trigger Rate: DC to 50 KHz.

Gate Delay 20 nS+(Delay Range)×(Control Voltage).

Delay Range: 1, 10, 100 or 1000 nS/Volt. (Control voltage input is on the rear.)

Delay Jitter: 2 pS rms.

Gate Width 100, 200, 500, or 1000 pS.

Gate View N-type connector. Leading edge indicates when gate

opens. Accuracy ±50 pS with respect to signal out.

Risetime < 50 pS.

SIGNAL CHANNEL

Signal Input N-type connector. Characteristic impedance is

50 Ohms. Protected to 5 VDC. The full scale

input level equals the sensitivity setting.

Shot Noise 200 µV rms on 1000 pS gate (typical)

350 μ V rms on 500 pS gate 600 µV rms on 200 pS gate

 $800 \, \mu V$ rms on $100 \, pS$ gate. Sensitivity 0.1, 0.25 or 1.0 Volts full scale. Overrange LED

indicates signal greater than full scale.

Signal Out

The Signal In is passed to the Signal Out for termination, gate timing, and for special applications

such as time domain reflectometry.

OUTPUTS

Sample Out ±1 V full scale analog output. Linearized and latched

> representation of the signal input as sampled during the gate. Resolution is 1/2% of full scale. Output impedance <1 Ohm. 10 mA drive capacity.

Digital Out Rear panel 8-bit digital interface is addressed as two

bytes, an 8-bit data byte for amplitude, an 8-bit status byte for sign, gate width sensitivity, data ready, rate

error, and overrun status.

GENERAL SPECIFICATIONS

Power +24 V/100 mA, -24 V/120 mA, +12 V/180 mA.

About 8 Watts total.

Connectors Three N-type to BNC transitions are provided.

SR200 Gate Scanner Module

The SR200 is designed to automate the recovery of waveforms with the SR250 and SR255. A waveform is recorded by plotting the 'Average Output' vs. the 'Delay Multiplier' setting as the Delay Multiplier is slowly scanned. The SR200 module will scan the delay multiplier (to scan the sample gate through the waveform) and control an X-Y chart recorder, strip chart recorder or oscilloscope.

The SR200 provides delay control for the SR255 and overrides the delay multiplier dial on the SR250. The SR200 electronically scans the delay multiplier over a range specified by 10 turn dials on its front panel. Single or repeated scans may be done in the forward or reverse direction over any portion of the waveform.



SPECIFICATIONS

CONTROLS

Reverse/Stop/Forward Selects the scan direction or stops the scan. Single/Reset/Repeat Selects single or repeated scans or resets to start. Scan Time

Selects time to complete one scan.

10 msec to 5 minutes.

Start Position Specifies the smallest Delay Multiplier in the scan. Scan Width Specifies the range of Delay Multipliers in the scan.

INDICATORS

Over Range LED Indicates if the delay multiplier exceeds 10.0.

Scanning LED Indicates that a scan is in progress.

Scan Complete LED Indicates when a single scan has been completed.

OUTPUTS

Control Voltage Rear panel output connects to the SR250 or SR255

> External Delay Multiplier Input. This output has an output impedance of less than 1 Ohm and current

limits at 20 mA.

Pen Lift Logic Signal to lift chart recorder pen or blank an

oscilloscope trace.

X-Axis Analog voltage output scans between 0 and

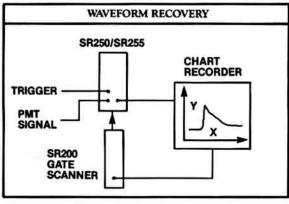
10.0 VDC regardless of the start position and scan

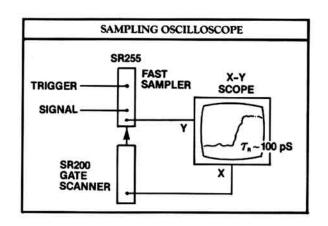
width dial settings.

GENERAL SPECIFICATIONS

Power Supplies +24 V/20 mA, +12 V/60 mA, -12 V/0 mA,

-24 V/20 mA. 2 Watts total.





SR235 Analog Processor Module

Often, additional processing of a Gated Integrator output is needed in an experiment. For example, in pulsed laser experiments, one may wish to normalize a laser-induced signal to the laser's intensity, and so eliminate the noise introduced by the laser's intensity fluctuations. Many other types of analog processing may be needed in other experiments.

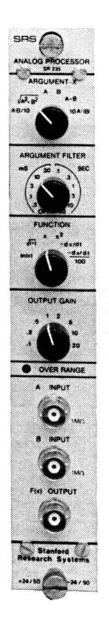
The SR235 Analog Processor is a convenient and flexible instrument which is capable of a wide variety of operations. The Analog Processor module provides an analog output F(x) which is formed from its analog inputs A and B. The

argument, x, can be A, B, A–B, A×B, A/B or $\sqrt{A^2+B}$. The argument may be filtered with a time constant from 0.3 mS to 30 S, or left unfiltered. The function may be any of x, x², \sqrt{x} , $\ln(x)$, dx/dt or (dx/dt)/100. Finally, an output gain from 0.1 to 20 may be selected. The result, 5 $\ln(10A/B)$ for example, is available at the output.

The Instrument may be used to normalize Boxcar outputs, find peaks in experimental scans, linearize exponential decay curves, compress analog signals in order to increase dynamic range, or simply to amplify a signal.

FEATURES

- 36 functions
- Gain Control
- Averaging of products and ratios
- Noise Reduction
- Normalization
- 2% Basic Accuracy



SPECIFICATIONS

A and B Inputs

Argument X

Filter

Function

Gain Select

F(x) Output

Frequency Response

Accuracy

Power

Input impedance of 1 M Ohm. Operating range of ±10 VDC, protected to 100 VDC. Input offset voltage is less than 2 mV.

Select A, B, $\sqrt{A^2+B^2}$, A-B, A×B/10 or 10A/B.

Select time constants from 0.3 mS to 30 S or none.

Select x, x^2 , \sqrt{x} , $\ln(x)$, -dx/dt or -(dx/dt)/100.

Selectable gains of 0.1 to 20 in a 1,2,5 sequence.

±10 VDC linear range. Output impedance is less than

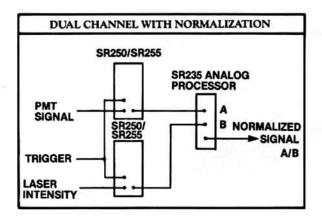
1 Ohm. Short circuit limits at 20 mA.

dx/dt to 10 Hz, (dx/dt)/100 to 1 KHz, all other from

DC to 50 KHz.

Gain 2%; Vector Sum 3%; Difference 1%; Multiplication 2% of full scale; Division (with denominator >0.1) 3% of full scale; $\ln(x)$, x^2 , and \sqrt{x} are accurate to ± 20 mV referenced to the input or at the output, whichever is less; dx/dt and (dx/dt)/100

+24/120 mA, -24/80 mA. 5 Watts total.



SR245 Computer Interface Module

The SR245 Computer Interface module is a powerful addition to your data acquisition capabilities. The unit provides both an analog and a digital interface between your computer and your experiment.

The eight analog I/O channels can be designated as inputs, outputs, or a combination, under software control. Both inputs and outputs have 13 bits of resolution over ±10.24 VDC full scale range, and 0.05% accuracy.

Two digital I/O bits are provided on the front panel which may be used as counters, triggers, or may be set or read by your computer. In addition, an 8-bit input and an 8-bit output port are available on an internal connector for your own custom digital interfaces.

Both RS-232-C and IEEE-488 interfaces are included for connection to your computer. The module is simple to control from high level languages. For example, sending ?5 instructs the module to digitize and send (in ASCII) the voltage on the 5th analog input BNC. Other commands allow you to record scans in the module's buffer memory, or ramp an analog output at a specified rate (for gate scanning), or read the contents of a digital counter.

FEATURES

Eight analog I/O Ports

- 18 digital I/O Bits
- RS-232-C and IEEE-488
- 3500 Sample Memory
- Counter Channel
- IBM Software Available

SPECIFICATIONS

ANALOG PORTS

Inputs

Any number of the eight ports may be designated under program control as input ports, the rest will

become output ports.

1 Megaohm input impedance, ±10.24 VDC range, protected to 40 VDC. 13-bit resolution (2.5 mV). Accuracy: 0.05%. Input offset less than 2.5 mV.

Maximum A/D rate is 2 KHz.

Outputs Output impedance less than 1 Ohm. Short circuit

current limit is 20 mA. 13 bit resolution (2.5 mV). Accuracy: 0.05%. Output offset less than 2.5 mV.

DIGITAL PORTS Front Panel BNC digital bits may be configured as

inputs or outputs under program control.

Front Panel Input impedance greater than 100 Kohms. Minimum Input Bits pulse width is 200 nS. Maximum count rate is 4 MHz.

Logic >3 VDC. Logic zero <0.7 VDC. Inputs

protected to ±10 VDC.

Can drive loads up to 50 Ohms to TTL logic levels. Output Bits

Internal 20 8 latched TTL output bits with strobe bit. Pin Connector 8-bit TTL input port with strobe bit.

INTERFACES Both IEEE-488 Std Port and RS-232-C (110 to 19.2 Kbaud). An Activity LED indicates when the unit is triggered, or when data is sent or commands received

over the interfaces. The error LED indicates an

overrange input or a bad command.

Power +24/60 mA, -24/60 mA, +12/400 mA, -12/20 mA.

Approximately 8 Watts total.

- 12 bit+sign resolution

FRACA

ACTIVITY

Abridged Command List

MR Master reset.

An,m

In Designates first n analog ports as inputs.

Returns the voltage at the nth analog port. ?n

?Bn Returns the logic level at the nth digital port.

?D Returns the value at the 8-bit digital input port.

?C Returns the pulse count at the 2nd digital input.

Sets the nth analog port to v volts.

SBn=m Set the nth digital bit high (m=1) or low (m=0).

SD=m Set the 8-bit digital output port to m.

SM=m Set the GPIB service request mask to m.

 T_n Trigger on every nth pulse at the sync port.

SCi,j,.:n Record analog ports i,j,.. for n triggers.

N Send one data point from the stored scan.

X Send all data points from the stored scan in binary.

(Provides ramp for waveform recovery.)

Add $n \times 2.5$ mV to the voltage at port 8 on every nth trigger.

SR280 System Mainframe and Display Module

The SR280 is the Boxcar Averager System Mainframe. The Mainframe is NIM (Nuclear Instrumentation Module) compatible, which allows modules from other manufacturers to be used in the SRS system leaving nine NIM slots available. The three right-most slots are filled by the display module and by the unregulated power supplies. The DC power supply regulators are mounted on a heat sink on the rear of the mainframe.

The Display Module features three types of display meters. The analog meter is for 'peaking-up' an experimental signal. The digit voltmeter allows accurate measurements to be made. The 'Digital Hold' button may be used to hold the digital meter's reading. A 20-segment bargraph display meter may be used to show rapidly changing data. The Display Module is available separately for use in other mainframes (Model SR275).

GENERAL SPECIFICATIONS

Power Mains 115 or 230 VAC (50/60 Hz). The power lines

are fused with 2A/IA for 115/230 VAC.

The 115 VAC bin supply has a 1 Amp fuse.

Mechanical NIM-compatible chassis, power supplies and

busses. Nine NIM slots are available. The mainframe may be rack mounted (19.5"), but also has feet for tabletop use.

Dimensions: 16.875" x 8.714" x 13.0".

DC Power ±12 VDC at 2A

±24 VDC at 1A

120 VAC is wired to each slot.

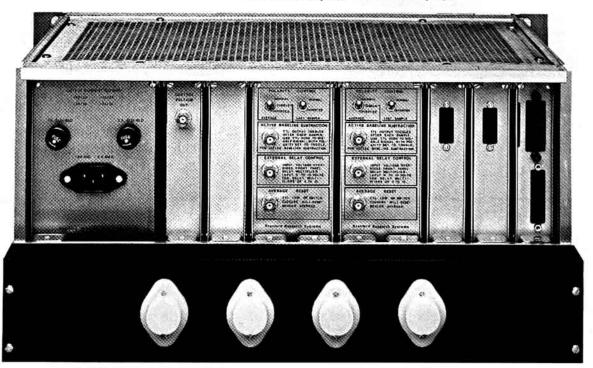
Display Module Analog meter 2% accuracy. ±10 VDC.

Zero center.

Digital Meter Bargraph

0.25% accuracy. 31/2 digit. ±10 VDC. 2% accuracy. 5% resolution. 20 segments. 50 KHz bandwidth. 0-10 V display.

-10 to +10 V display. -10 to 0 V display.



Rear view of the SR280 Mainframe, Gate Scanner, Analog Processor, two Boxcar Modules, two Fast Samplers, and a Computer Interface.



STANFORD RESEARCH SYSTEMS

1290-D Reamwood Avenue, Sunnyvale, CA 94089 Telephone (408)744-9040, Fax (408)744-9049

email: info@thinkSRS.com Web: www.thinkSRS.com